

### REMARKS

An RCE application accompanies this submission, so entry and earnest consideration of the foregoing amendments are respectfully requested. Claims 2-4 and 13-32 have been canceled from this application. Claims 1, 5, 6, 7, 8 and 9 were rejected under 35 U.S.C. 103(a) as allegedly unpatentable over Hedge et al (US 6,717,226) in view of Gardner et al (US 6,020,260). Claims 1, 5-7, 8-9, and 11-12 were rejected under 35 U.S.C. 103(a) as allegedly unpatentable over Paton et al (US 6,682,973) in view of Gardner. Claim 20 was rejected under 35 U.S.C. 103(a) as allegedly unpatentable over Paton et al in view of Gardner further in view of Yu et al (US 6,573,193).

Applicant has amended independent claim 1 and added new claims 33-34 to more clearly identify novel and non-obvious aspects of embodiments of the invention. Support for the amended and newly added features can be found throughout the specification, drawings and claims of the original application. Accordingly, no new matter is added to the application by this submission.

#### Claim 1

Among other features, claim 1 recites a step of "forming a silicon-containing electrode layer over the metal oxide layer *by depositing a silicon layer and introducing a nitrogen containing ambient simultaneously*" (*Emphasis added*). The Office Action admits that Hedge et al. and Paton et al. do not explicitly teach that the polysilicon electrode is formed in a nitrogen containing ambient, but alleges that Gardner teaches that a polysilicon electrode is formed in a nitrogen containing ambient (see col. 2 lines 34-41). Applicant respectfully disagrees.

Instead, Applicant respectfully submits that Gardner discloses “the lower polysilicon layer is formed by depositing a layer of polysilicon in an amorphous state and *annealing the amorphous polysilicon layer* in a nitrogen bearing ambient (*Emphasis added*). More specifically, an *amorphous polysilicon layer* is deposited first. The *amorphous polysilicon layer* is annealed in a nitrogen bearing ambient subsequently. The annealing procedure disclosed by Gardner is a post heat treatment after the amorphous polysilicon layer is formed. Significantly, Gardner fails to teach or suggest forming a silicon-containing electrode layer over the metal oxide layer *by depositing a silicon layer and introducing a nitrogen containing ambient simultaneously* explicitly. Moreover, the polysilicon electrode layer disclosed by Gardner is formed on silicon oxide, while the polysilicon electrode layer taught by Hedge and Paton is formed on the metal oxide with high dielectric constant. Consequently, there is no proper motivation to combine Hedge and Gardner or to combine Paton and Gardner, since the interface properties of the polysilicon-silicon oxide interface and the polysilicon-metal oxide interface are different.

It is therefore respectfully submitted that neither Hedge et al. nor Paton et al. nor Gardner et al., singly or combined, teach or properly suggest forming a silicon-containing electrode layer over the metal oxide layer *by depositing a silicon layer and introducing a nitrogen containing ambient simultaneously* explicitly.

For at least this reason, claim 1 (as amended herein) patentably defines over the cited art of record. As claims 5-12 directly or indirectly depend from amended claim 1, claims 5-12 are patentable by virtue of their dependency from patentable claim 1.

Claim 33

Newly added claim 33 recites a step of “*depositing* a polysilicon electrode over the metal oxide layer by a low pressure chemical vapor deposition (LPCVD) process *simultaneously in association with a nitrogen containing ambient*” (*Emphasis added*). The Office Action admits that Hedge et al. and Paton et al. do not explicitly teach that the polysilicon electrode is formed in a nitrogen containing ambient.

Applicant respectfully submits that Gardner discloses “the lower polysilicon layer is formed by depositing a layer of polysilicon in an amorphous state and *annealing the amorphous polysilicon layer* in a nitrogen bearing ambient (*emphasis added*). More specifically, an *amorphous polysilicon layer* is deposited first. The *amorphous polysilicon layer* is annealed in a nitrogen bearing ambient subsequently. The annealing procedure disclosed by Gardner is a post heat treatment after the amorphous polysilicon layer is formed. Gardner fails to teach or suggest *depositing* a polysilicon electrode over the metal oxide layer by a low pressure chemical vapor deposition (LPCVD) process *simultaneously in association with a nitrogen containing ambient*.

For at least this reason, newly added claim 33 is patentable. As claim 34 directly or indirectly depends from claim 33, claim 34 is patentable by virtue of its dependency from patentable claim 33.

CONCLUSION

For at least the reasons set forth above, Applicant respectfully submits that all objections and/or rejections have been traversed, rendered moot, and/or accommodated, and that the now pending claims are in condition for allowance. Favorable reconsideration and allowance of the present application and all pending claims are hereby courteously requested. If, in the opinion of

the Examiner, a telephonic conference would expedite the examination of this matter, the Examiner is invited to call the undersigned attorney at (770) 933-9500.

A credit card authorization is provided herewith to cover the fees associated with the filing of the RCE and the required time extension. No additional fee is believed to be due in connection with this amendment and response to Office Action. If, however, any additional fee is believed to be due, you are hereby authorized to charge any such fee to deposit account No. 20-0778.

Respectfully submitted,

  
 Daniel R. McClure; Reg. No. 38,962

**THOMAS, KAYDEN, HORSTEMEYER & RISLEY, L.L.P.**  
 Suite 1750  
 100 Galleria Parkway N.W.  
 Atlanta, Georgia 30339  
 (770) 933-9500